Amendments to the Claims

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A digital data recovery circuit for converting an input signal into a sliced signal comprising:

a comparing device coupled with the input signal and a reference level signal for comparing the input signal with the reference level signal and generating the sliced signal having a first binary value and a second binary value according to the result of comparison, wherein the sliced signal keeps at the first binary value for a first time period and keeps at the second binary value for a second time period;

a phase-detecting, level-determining device coupled with the comparing device, wherein the phase-detecting, level-determining device is for detecting ~~the~~ a relation between the first time period and the second time period ~~phase at which the transition of the sliced signal occurs~~, based on a reference clock, and for generating a digital level signal according to the result of detection; and

a digital-to-analog converter (DAC) coupled with the phase-detecting, level-determining device for generating the reference level signal for the comparing device according to the digital level signal.

2. (currently amended) The digital data recovery circuit of claim 1 wherein the phase-detecting, level-determining device further comprises:

a phase detector coupled with the comparing device for detecting the relation between the first time period and the second time period by detecting [[the]] a phase of the sliced signal transiting from [[a]] the first binary value to [[a]] the second binary value[[,]] and [[the]] a phase of the sliced signal transiting from the second binary value to the first binary value, based on the reference

clock; and

a level determiner coupled with the phase detector for generating the digital level signal according to the result of detection.

3. (original) The digital data recovery circuit of claim 2 wherein the phase detector comprises:

N flip-flop series wherein each of the flip-flop series has an input end, a clock input end, and an output end, and each input end of the flip-flop series is coupled with the sliced signal with the clock input end of a K^{th} flip-flop series being coupled with the signal generated by delaying the reference clock for K/N period; and

N transition phase detecting devices wherein each transition phase detecting device has a first input end, a second input end, a first output end, and a second output end; the first input end of an L^{th} transition phase detecting device is coupled with the output end of the L^{th} flip-flop series, the second input end of the L^{th} transition phase detecting device coupled with the output end of an $L+1^{th}$ flip-flop series, the first input end of an N^{th} transition phase detecting device coupled with the output end of an N^{th} flip-flop series, and the second input end of the N^{th} transition phase detecting device coupled with the output end of the first flip-flop series,

wherein N is a positive integer, K is a positive integer between 1 and N, and L is a positive integer between 1 and N-1.

4. (original) The digital data recovery circuit of claim 3 wherein the K^{th} flip-flop series comprises M cascaded flip-flops, and the clock input end of each flip-flop is coupled with the clock input end of the K^{th} flip-flop series, the input end of a first flip-flop is used as the input end of the K^{th} flip-flop series, the output end of an M^{th} flip-flop is used as the output end of the K^{th} flip-flop series, and when M is larger than 1, the output end of a P^{th} flip-flop is coupled with the input end of a $P+1^{th}$ flip-flop where M is a positive integer and P is a positive integer between 1

and M-1.

5. (original) The digital data recovery circuit of claim 3 wherein an R^{th} transition phase detecting device comprises:

an upward transition detecting unit comprising a first input end coupled with a first input end of the R^{th} transition phase detecting device, a second input end coupled with a second input end of the R^{th} transition phase detecting device, and an output end used as a first output end of the R^{th} transition phase detecting device; and

an downward transition detecting unit comprising a first input end coupled with a first input end of the R^{th} transition phase detecting device, a second input end coupled with a second input end of the R^{th} transition phase detecting device, and an output end used as a second output end of the R^{th} transition phase detecting device,

wherein R is a positive integer between 1 and N.

6. (original) The digital data recovery circuit of claim 5 wherein the upward transition detecting unit of the R^{th} transition phase detecting device comprises:

a first inverter with its input end used as the first input end of the upward transition detecting unit; and

a first AND gate with its input end coupled with an output end of the first inverter, another input end used as the second input end of the upward transition detecting unit, and an output end used as the output end of the upward transition detecting unit.

7. (original) The digital data recovery circuit of claim 5 wherein the downward transition detecting unit of the R^{th} transition phase detecting device comprises:

a second inverter with its input end used as the second input end of the downward transition detecting unit; and

a second AND gate with its input end coupled with an output end of the second

inverter, another input end used as the first input end of the downward transition detecting unit, and an output end used as the output end of the downward transition detecting unit.

8. (original) The digital data recovery circuit of claim 5 wherein the upward transition detecting unit of the R^{th} transition phase detecting device comprises:

a first inverter with its input end used as the second input end of the upward transition detecting unit;

a first OR gate with its input end coupled with an output end of the first inverter and another input end used as the first input end of the upward transition detecting unit; and

a second inverter with its input end coupled with an output end of the first OR gate, and an output end used as the output end of the upward transition detecting unit.

9. (original) The digital data recovery circuit of claim 5 wherein the downward transition detecting unit of the R^{th} transition phase detecting device comprises:

a third inverter with its input end used as the first input end of the downward transition detecting unit;

a second OR gate with its input end coupled with an output end of the third inverter and another input end used as the second input end of the downward transition detecting unit; and

a fourth inverter with its input end coupled with an output end of the second OR gate, and an output end used as the output end of the downward transition detecting unit.

10. (original) The digital data recovery circuit of claim 2 wherein the phase detector is in a delay locked loop.

11. (original) The digital data recovery circuit of claim 1 wherein the comparing

device is a comparator generating the sliced signal having the first binary value when the level of the input signal is lower than the level of the reference level signal and generating the sliced signal having the second binary value when the level of the input signal is higher than the level of the reference level signal.

12. (original) The digital data recovery circuit of claim 1 wherein the comparing device is an one-bit analog-to-digital converter (ADC) generating the sliced signal having the first binary value when the level of the input signal is lower than the level of the reference level signal and generating the sliced signal having the second binary value when the level of the input signal is higher than the level of the reference level signal.

13. (original) The digital data recovery circuit of claim 1 wherein the comparing device is an ADC generating the sliced signal with bit values from 1 to N according to the relationship between the input signal and the reference level signal.

14. (original) The digital data recovery circuit of claim 1 wherein the comparing device is a partial-response maximum likelihood circuit generating the sliced signal having the first binary value when the level of the input signal is lower than the level of the reference level signal and generating the sliced signal having the second binary value when the level of the input signal is higher than the level of the reference level signal.

15. (original) The digital data recovery circuit of claim 1 wherein the DAC is a voltage source for providing a reference level required by the comparing device.

16. (original) The digital data recovery circuit of claim 1 wherein the DAC is a current source for providing a reference level required by the comparing device converted by an external circuit from a current generated by the DAC.

17. (original) The digital data recovery circuit of claim 1 wherein the DAC is a control circuit for directly controlling the bit value of the sliced signal output by the comparing device.